Piecewise BJT Process Spread Compensation Exploiting Base Recombination Current

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***Abstract*—In this paper, a piecewise bipolar junction transistor (BJT) process spread compensation scheme is presented. By exploiting the strong correlation between the BJT saturation current and the piecewise base recombination current, the process spread and proportional-to-absolute-temperature (PTAT) drift of the base–emitter voltage (V_{be}) can be reduced over a wide temperature range. Fabricated in standard 0.18-µm CMOS, the chip prototype achieves a measured V_{be} standard deviation (STD) of 1.1 mV (1.8 mV) from -30 to 60 °C (-30 to 120 °C) over 12 samples, corresponding to a 2.9X (1.8X) improvement when compared to the measured V_{be} STD of 3.24 mV at 25 °C from 15 standalone BJT samples with constant external bias current using the same process.**

Keywords—Bipolar junction transistor (BJT), piecewise process spread compensation, base recombination current.

I. Introduction

Bipolar junction transistors are used widely in CMOS bandgap references and temperature sensors [1]-[3]. However, the reproducibility of the base-emitter voltage V_{be} of the BJT ultimately limits the achievable precision in such systems [4]. In general, a trimming circuit is required to tackle process variations, with the penalties of increased circuit complexity, chip area and production cost.

The sources of variations in V_{be} come from random dopant fluctuations, lithographic limits and electrical environment variations [4]. Various attempts have been made to accomplish high precision V_{be} without trimming by exploiting the correlations between device parameters. In [5], the correlation between the BJT saturation current I_S and its forward current-gain β_F is explored. The variation in V_{be} can be compensated by placing a resistor in series with the BJT base to extract β_F. In [6], the correlation between a pinched resistor and I_S is exploited to reduce the spread of V_{be}. However, pinched resistors are not widely supported in modern CMOS processes. In [7], the strong correlation between I_S and reverse current gain β_R was exploited to reduce the PTAT spread in V_{be}. Recently, a compensation method exploiting the correlation between I_S and base recombination current was proposed [8]. Even though this approach can achieve a V_{be} STD of as low as ~1 mV, it can only achieve single-point optimization and exhibits limitations in effective V_{be} compensation over different temperature.

This paper proposes a piecewise BJT process spread compensation scheme over a wide temperature range from -30 to 120 °C. By exploiting the recombination current generated by a deep saturated BJT and piecewise compensation at different temperatures, the measured STD of V_{be} can be reduced to 1.8 mV from -30 to 120 °C over 12 samples, corresponding to a 1.8X improvement when compared to the measured V_{be} STD of 3.24 mV from 15 standalone BJT samples without compensation using the same process. The measured V_{be} STD is 1.1 mV from -30 to 60 °C, demonstrating a 39% error reduction when compared with [8].

II. Operating Principles

For a BJT, the base-emitter junction voltage (V_{be}) is defined as [4]

$$V_{be} = \frac{kT}{q} ln\left(\frac{I_c}{I_s}\right), \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, and I_c and I_s are the BJT collector and saturation currents, respectively. The temperature characteristics of V_{be} mainly depends on I_s, which is defined as

$$I_S = \frac{qAn_i^2\overline{D_n}}{W_b N_b}, \tag{2}$$

where n_i is the intrinsic carrier concentration, $\overline{D_n}$ is the average diffusion constant of minority carriers in the base, W_b is the base width and N_b is the base doping concentration. As a result, I_s suffers from process variation, and consequently leads to a spread in V_{be}. If I_s exhibits a variation ΔI_s from its nominal value, by assuming $\Delta I_s \ll I_s$,

$$V_{be} \approx \frac{kT}{q} ln\frac{I_c}{I_s} + \frac{kT}{q}\frac{\Delta I_S}{I_S}, \tag{3}$$

where the first and second terms denote the nominal value and spread of V_{be}, respectively. It can be observed that the spread in V_{be} increases with temperature, and can result in $\pm$30% inter-/intra-die variation in I_S, which can lead to a spread of 10.5 mV in V_{be} at 125 ℃.

In [8], a BJT process spread compensation method which exploits the correlation between I_s and the recombination current is proposed. It demonstrates that a BJT working in the deep saturation region can be used for I_s spread compensation

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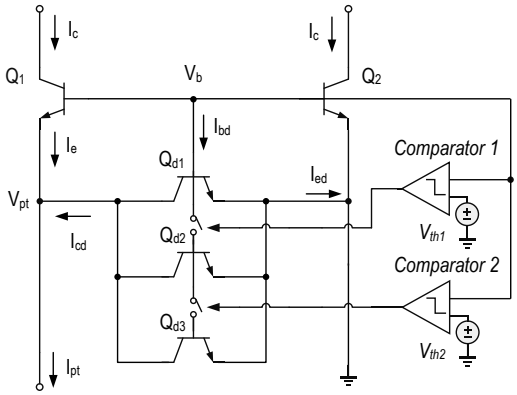

Fig. 1. The basic concept of the proposed piecewise BJT process compensation scheme. The emitter ratio of Q_1, Q_2, Q_{d1}, Q_{d2} and Q_{d3} is 4:2:4:1:1.

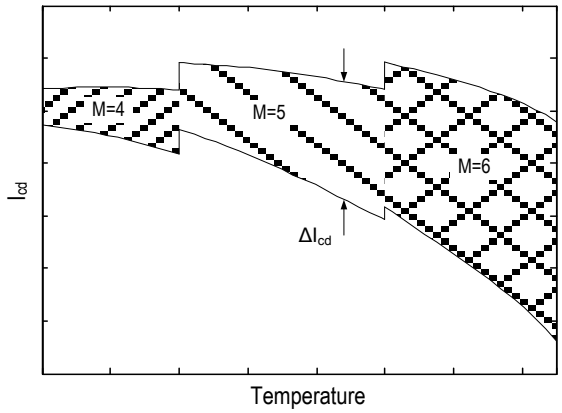

Fig. 2. Illustrative compensation current I_{cd} from a BJT with M = 4, 5, 6 respectively. The spread of compensation current ΔI_{cd} (upper and lower bound) increases with increasing M for a given ΔI_S. The shaded area shows the combined effective compensation region.

if its recombination current satisfies two requirements: 1) it exhibits strong correlation with I_s; and 2) its spread also increases with temperature to compensate for the temperature dependency of I_S. The recombination current I_r can be expressed as [8]

$$I_r = \frac{Q_n}{\tau_b} \approx \frac{AqW_b{n_i}^2}{2N_b\tau_b}\left(e^{V_{be}/V_T} + e^{V_{bc}/V_T}\right), \quad (4)$$

where τ_b is the minority carrier life time, A is the BJT emitter area, and $V_T = kT/q$ is the thermal voltage. It can be deduced that $I_r \propto \tau_b^{-1}$. Based on the concentration-dependent Shockley-Read-Hall (SRH) model, as $\tau_b \propto N_b^{-1}$ for $N_b \geq 10^{17}/\text{cm}^3$ [9], $I_r \propto N_b$. Since $I_S \propto N_b^{-1}$, $I_r \propto I_s^{-1}$ and this strong correlation can be utilized to compensate for the process variation of I_s. Yet, this optimization process is design dependent and can achieve effective process compensation of I_s only within a narrow temperature range [8].

To tackle this problem, this work proposes a piecewise BJT process spread compensation scheme over a wide temperature range. Fig. 1 shows the proposed piecewise BJT process compensation scheme. $Q_{1,2}$ of different sizes are biased with the same collector current. Q_d is the compensation BJT biased in its deep saturation region, whose collector current I_{cd} (containing the recombination current I_r) flows into V_{pt}. As a result, the voltage V_b becomes process compensated. To achieve effective process compensation in I_s over a wide temperature range, the variation of I_{cd} (i.e. ΔI_{cd}) should be complementary-to-absolute-temperature (CTAT). According to the Ebers-Moll model, I_{cd} can be expressed as

$$I_{cd} = MI_s\left(e^{V_{be}/V_T} - 1\right) - \frac{MI_S}{\alpha_R}\left(e^{V_{bc}/V_T} - 1\right), \quad (5)$$

and its deviation with respect to temperature is

$$\frac{\partial I_{cd}}{\partial T} = \frac{M}{TV_T}\left[\frac{I_s}{\alpha_R} \cdot e^{V_{bc}/V_T} \cdot V_{bc} - I_s \cdot e^{V_{be}/V_T} \cdot V_{be}\right]. \quad (6)$$

where M is the emitter area ratio between Q_d, and a unit BJT, and α_R is the reverse current gain. Similarly,

$$\Delta I_{cd} = M\left[\Delta I_s\left(e^{V_{be}/V_T} - 1\right) - \frac{\Delta I_S}{\alpha_R}\left(e^{V_{bc}/V_T} - 1\right)\right], \quad (7)$$

with

$$\frac{\partial \Delta I_{cd}}{\partial T} = \frac{M}{TV_T}\left[\frac{\Delta I_S}{\alpha_R} \cdot e^{V_{bc}/V_T} \cdot V_{bc} - \Delta I_s \cdot e^{V_{be}/V_T} \cdot V_{be}\right]. \quad (8)$$

For a given $\Delta I_s > 0$, it can be observed that both (6) and (8) can be negative if

$$V_{ce} > V_T \cdot ln\left(\frac{V_{bc}}{V_{be} \cdot \alpha_R}\right). \quad (9)$$

The CTAT characteristics of ΔI_{cd} can be utilized to compensate for the positive temperature dependency of ΔI_S [4] for a particular chip. It can be observed that the compensation strength for I_{cd}, ΔI_{cd} and their temperature dependencies can be controlled by M. Due to the difficulty in achieving simultaneous optimal compensation for both process and temperature with a fixed M, effective process compensation can only be achieved in a narrow temperature range. Notice that both I_{cd} and ΔI_{cd} are proportional to M. As M increases, $\partial \Delta I_{cd}/\partial T$ becomes more negative, which means that a BJT with different M can achieve different process and temperature compensation characteristics. This property can be exploited to achieve BJT process compensation over a wide temperature range, as shown in Fig. 2 with M equals to 4, 5 and 6, respectively. Within each temperature range, the V_b spread due to I_s is compensated by the corresponding I_{cd}. Since ΔI_{cd} increases as M increases, the required compensation strength over a wide temperature range can be well controlled to counteract the PTAT spread of V_b as a result of the temperature dependency of ΔI_S.

To achieve reconfiguration of M at different temperature range, a selection circuit which is formed by the two comparators as shown in Fig. 1 is required to change M between 4, 5 and 6. The selection of M can achieved by comparing V_b with predefined threshold voltages (corresponding to different switching temperatures). Fig. 3 shows the simulated STD of V_b with different emitter areas of Q_d from 250 Monte-Carlo simulation runs using the proposed compensation scheme. It can be observed that an optimal M

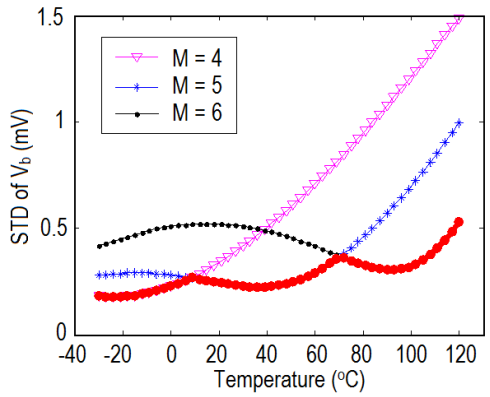

Fig. 3. Simulated STD of V_b with three different compensation strengths over different temperature range from 250 Monte-Carlo runs.

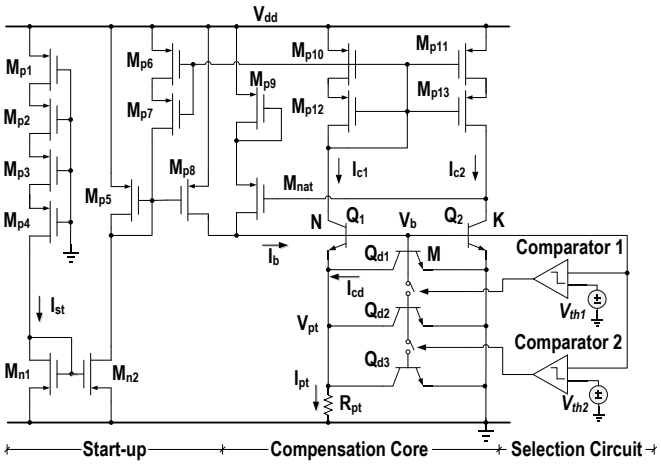

Fig. 4. Schematic of the proposed piecewise BJT process compensation circuit.

exists to achieve the lowest STD of V_b at different temperatures. By using piecewise compensation through controlling M, a simulated V_b STD of less than 0.4 mV can be achieved from -30 to 60 °C. This value gradually increases up to ~0.6 mV at 120 °C.

III. Implementation of the Proposed Piecewise BJT Process Compensation Circuit

Fig. 4 shows the implementation of the complete piecewise BJT process compensation circuit. $M_{p1\text{-}8}$ and $M_{n1,2}$ form the start-up circuit. $M_{p9\text{-}13}$ and a native transistor M_{nat} generate the bias current for the BJTs. The two comparators evaluate the difference between V_b and $V_{th1,2}$, then generate the control signals to change M by turning on/off the corresponding $Q_{d2,3}$.

As on-chip resistors also suffer from process spread as a result of the variation in the doping concentration and diffusion depth, this can vary the value of I_{pt}, which can directly affect the effectiveness of the proposed compensation scheme. Since the spreads of different resistors originate from independent physical sources, we can reduce their effective variation by combining different resistor types to form a composite resistor [10]. In the selected 0.18-µm CMOS process, R_{pt} of 220 kΩ is composed of weighted combinations of 6 different types of resistors, with their individual simulated normalized STD as shown in Table I. The simulated maximum STD of R_{pt} is 5.1 kΩ at 120 °C. This corresponds to a normalized STD of 2.28%, which is more than 57% lower when compare to any single-type resistors.

The BJT core contains the main BJTs $Q_{1,2}$ and the compensation BJTs $Q_{d1,2,3}$. $Q_{1,2}$ work in their forward-active regions, while $Q_{d1,2,3}$ work in the deep saturation region (with their V_{ce} equals to 25 mV at 120 °C). The emitter area ratio of $Q_{1,2}$ is set to 4:2. Even though V_{pt} is process independent, I_{pt} still suffers from the process spread of R_{pt} (STD = 2.28% in simulation), with a nominal value of 85 nA at 27 °C. Since this process compensation circuit is sensitive to mismatch, common-centroid layout technique and dummies are used to reduce the mismatch of BJTs.

TABLE I. Components of The Composite Resistor

Resistor Type	Normalized STD[a]	Percentage
Unsalicide N+ diffusion resistor	5.5%	25%
Unsalicide N+ poly resistor	5.25%	25%
Unsalicide high sheet resistance N+ poly resistor	6.25%	20%
Unsalicide P+ diffusion resistor	8.5%	10%
Unsalicide P+ poly resistor	7.25%	15%
Salicide P+ poly resistor	15%	5%

[a] Normalized STD calculated from 50 Monte-Carlo runs.

As discussed before, the switch circuit consists of two comparators which compares with the predefined threshold voltages $V_{th1,2}$. The value of M is set to 4 for compensation at low temperature, and increases as V_b crosses V_{th1} and V_{th2} as temperature rises. The comparator offset can lead to variation in the switching point, leading to an increased STD in V_b. (can be as large as 0.5 mV in simulation). To alleviate this problem, the comparator offset is reduced by large input transistor size and careful layout to ensure good matching.

IV. Measurement Results

Fig. 5 shows the chip micrograph of the proposed compensation circuit fabricated in a standard 0.18-µm CMOS process, with an active area of 0.0448 mm^2. Fig. 6 shows the measured V_b of 12 dies at different temperatures, with the measured STD as shown in Fig. 7. It can be observed that when T<60 °C, the measured STD of V_b reduces to about 1.1 mV, which is 39% less than that achieved in [8]. For T >60 °C, the measured V_b STD is gradually increases to 1.8 mV at 120 °C, which is consistent with the simulation result as shown in Fig. 3. The residue error between simulation and measurement is mainly due to the BJT modeling limitations and resistor spread prediction in simulation. Apart from that, the mismatches among BJTs $Q_{1,2}$ and $Q_{d1,2,3}$, and that of $M_{p10,12}$ and $M_{p11,13}$ also affect the biasing condition, increasing the

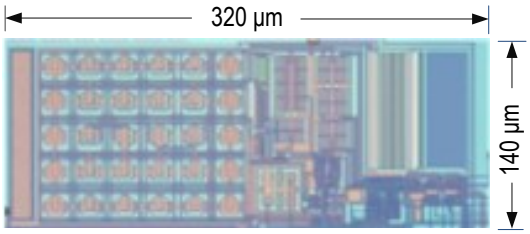

Fig. 5. Chip micrograph of the proposed compensation circuit.

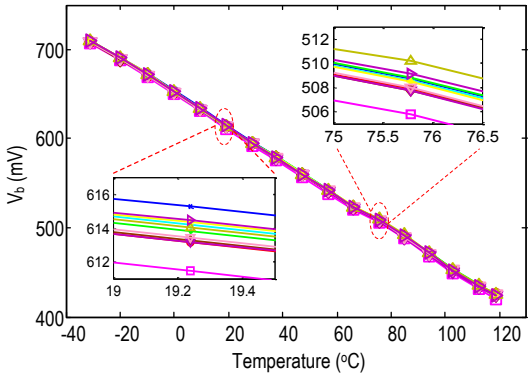

Fig. 6. Measured V_b of 12 dies at different temperatures, with zoom in at two switching points.

STD of V_b. It is worth mentioning that according to the measurement result, the maximum STD of V_b is 1.8 mV at high temperature, and can be further reduced by increasing I_{pt} through reducing R_{pt}. Table II shows the performance summary of the proposed piecewise BJT process compensation circuit. With a supply voltage of 1.2 V, the proposed compensation circuit achieves a measured V_{be} STD of 1.8 mV from -30 to 120 °C over 12 samples, corresponding to a 1.8X improvement when compared to the measured V_{be} STD of 3.24 mV from 15 standalone BJT samples without compensation using the same process. The measured V_{be} STD is 1.1 mV from -30 to 60 °C, demonstrating a 39% error reduction when compared with [8].

CONCLUSION

A piecewise BJT process compensation based on the BJTs base recombination current is presented. A deep saturated BJT with reconfigurable emitter area M is utilized to achieve optimal BJT process compensation result over a wide temperature range. This work obtains an average STD of V_b of 1.1 mV from -30 ℃ to 60 ℃, 1.5 mV from 60 ℃ to 110 ℃, and the maximum 1.8 mV at 120 ℃, demonstrating the effectiveness of the proposed technique for wide temperature range BJT process spread compensation.

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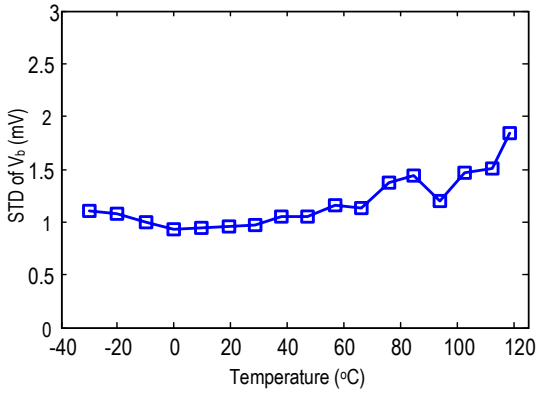

Fig. 7. Measured STD of V_b at different temperatures.

TABLE II. PERFORMANCE SUMMARY OF THIS WORK

Parameter		**This work**
CMOS process (μm)		0.18
Temperature Range (°C)		-30 ~120
Supply Voltage (V)		1.2
Current Consumption (nA)		635.5
Maximum STD of V_b (mV)	-30 ~ 60 °C	1.1
	60 ~ 120 °C	1.8
Chip Area (mm^2)		0.0448

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